WHAT IS CLAIMED IS:

1. A system for decreasing transmission timing variations comprising:

a gate circuit for inputting a precharging control signal and for generating an output driving signal in response to the control signal before a data bit is input; and

an output driver connected to a data channel and responsive to the output driving signal for precharging the data channel to a voltage level before the data bit is input.

2. The system of claim 1, wherein the control signal is enabled during a time period before the data bit is input.

3. The system as in claim 2, wherein the time period comprises a range of at least half a clock cycle to a full clock cycle.

4. The system of claim 1, wherein the gate circuit does not generate the output driving signal upon receiving a power down signal associated with a power down logic state.

5. The system of claim 1, wherein the output driver includes first and second transistors connected serially between the data channel and a ground voltage.

6. The system of claim 5, wherein the first transistor responds to an active signal having a voltage level before the data bit is input, and the second transistor is responsive to the output driving signal to precharge the data channel.

7. A system for decreasing transmission timing variations comprising:

an N-1 first gate circuit for inputting associated data bits and generating a first output driving signal in response to a first clock signal;

an N-1 output driver connected to a data channel and responsive to the first output driving signal;

an NTH gate circuit for inputting associated data bits and generating a second output driving signal in response to a second clock signal; and

an NTH output driver connected to the data channel and responsive to the second output driving signal,

wherein the second output driver is further responsive to a precharging control signal to precharge the data channel to a voltage level before a first data bit is input.

8. The system of claim 7, wherein the control signal is enabled during a time period of the first clock signal before the first data bit is input.

9. The system as in claim 8 wherein the time period comprises a range of at least half a clock cycle to a full clock cycle of the first clock.

10. The system of claim 7, wherein each of the gate circuits does not generate the respective output driving signal upon receiving a power down signal associated with a power down logic state.

11. The system of claim 7, wherein each of the output drivers includes transistors serially connected between the data channel and a ground voltage.

12. The system of claim 11, wherein one of the transistors responds to a signal having a voltage level before the first data bit is input, and the other transistor responds to the associated output driving signal.

13. A method for decreasing transmission timing variations comprising:

inputting a precharging control signal;

generating an output driving signal in response to the control signal before a data bit is input; and

precharging a data channel to a voltage level before the data bit is input using the output driving signal.

14. The method of claim 13, further comprising enabling the control signal during a time period before the data bit is input.

15. The method as in claim 14, wherein the time period comprises a range of at least half a clock cycle to a full clock cycle.

16. The method of claim 13, wherein the output driving signal is not generated when a power down signal associated with a power down logic state is received.

17. A method for decreasing transmission timing variations comprising:

inputting associated data bits and generating an N-1 output driving signal in response to a first clock signal;

inputting associated data bits and generating an NTH output driving signal in response to a second clock signal; and

precharging a data channel to a voltage level in response to a precharging control signal before a first data bit is input.

18. The method of claim 17, further comprising enabling the control signal during a time period of the first clock signal before the first data bit is input.

19. The method of claim 18, wherein the time period comprises a range of at least a half clock cycle to a full clock cycle of the first clock.

20. The method of claim 17, wherein no output driving signals are generated upon receiving a power down signal.

21. In a system comprising a gate circuit for inputting a precharging control signal and for generating an output driving signal in response to the control signal before a data bit is input and an output driver connected to a data channel and responsive to the output driving signal for precharging the data channel to a voltage level before the data bit is input, a method for decreasing transmission timing variations comprising:

inputting the precharging control signal;

generating the output driving signal in response to the control signal before a data bit is input; and

precharging the data channel to a voltage level before the data bit is input using the output driving signal.

22. In a system comprising an N-1 gate circuit for inputting associated data bits and generating a first output driving signal in response to a first clock signal, an N-1 output driver connected to a data channel and responsive to the first output driving signal, an Nth gate circuit for inputting associated data bits and generating a second output driving signal in response to a second clock signal and an NTH output driver connected to the data channel and responsive to the second output driving signal, wherein the second output driver is further responsive to a precharging control signal to precharge the data channel to a voltage level before a first data bit is input, a method for decreasing transmission timing variations comprising:

inputting the associated data bits and generating the N-1 output driving signal in response to the first clock signal;

inputting the associated data bits and generating the NTH output driving signal in response to the second clock signal; and

precharging the data channel to the voltage level in response to the precharging control signal before the first data bit is input.